PHASE LOCKED LOOP FILTER

The present invention relates to a phase locked loop filter.

Radiotelephone systems typically require low phase noise, fast switching times, and precise accuracy of the channel frequencies.

In order to design a PLL having the required characteristics (e.g. low phase noise) the associated PLL filter typically requires more than 10nF of capacitance, where the largest PLL capacitor will be the 'zero' capacitor (i.e. the PLL filter capacitor that is used to create a zero in the filters transfer function, which is necessary for the PLL's stability).

However, it can be difficult and costly to achieve single-chip integration for a PLL that requires such a large capacitance.

One technique that has been developed to reduce the required capacitance for a PLL, thereby allowing single-chip integration, while also retaining the same overall PLL transfer function (i.e. PLL loop dynamics), involves the use of a dual path PLL filter, in which each PLL filter path is driven by a separate charge pump path, for example from a charge pump having two output paths or two separate charge pumps having a single output path.

One example of dual path PLL filter was proposed by Craninckx and Steyaert, IEEE Journal of Solid-State Circuit, Vol. 33, No. 12, December 1998 in which a dual path PLL filter incorporated two active devices, an amplifier and a voltage adder.

Another example of a dual path PLL filter was proposed by Koo, IEEE Journal of Solid-State Circuit, Vol. 37, No. 5, May 2002 in which a dual path PLL filter incorporated a single active device, an amplifier.

However, the use of active devices within a PLL filter increases both phase noise and power consumption as well as increasing the complexity of the PLL filter.

US 5,774,023 discloses a loop filter that includes a high current first pole filter capacitor, a high current first pole damping resistor, a low current first pole filter capacitor, a low current first pole damping resistor and a first pole filter capacitor in which the loop filter is driven by a first charge pump output when current pulses from the charge pump are commensurate with a final narrow loop bandwidth otherwise the loop filter is driven by a second charge pump output. As such US 5,774,023 discloses the switching of current source between the first charge pump output and the second charge pump output rather than simultaneous output.

According to an aspect of the present invention there is provided a phase locked loop filter according to claim 1.

This provides the advantage of allowing a loop filter capacitance to be integrated onto a single chip without requiring the use of an active component, for example a voltage adder or an integrator.

An embodiment of the invention will now be described, by way of example, with reference to the drawings, of which:

Figure 1 illustrates a phase locked loop incorporating a filter according to an embodiment of the present invention;

Figure 2 illustrates a phase locked loop filter according to an embodiment of the present invention;

Figure 3 shows graphs illustrate dual path characteristics of a phase locked loop filter according to an embodiment of the present invention;

Figure 4 illustrates a graph showing the phase noise characteristics of a phase locked loop filter according to an embodiment of the present invention.

Figure 1 illustrates a phase locked loop 10 for use in a radiotelephone (not shown). The phase locked loop 10 incorporates a phase detector 11 having a first input for receiving a reference frequency, a second input for receiving a PLL loop frequency and an output for coupling to a charge pump 12. The charge pump 12 has two output paths that are coupled to respective input paths of a loop filter 13. The loop filter 13 is coupled to a voltage controlled oscillator VCO 14. The VCO 14 is coupled to a first x2 divider 15, which provides an input to both a DCS portion of the radiotelephone and to a second x2 divider 16. The second x2 divider 16 provides an input to both a GSM portion of the radiotelephone and to an N divider 17. The N divider 17 is coupled to the second input of the phase detector 11 for providing the PLL loop frequency to the phase detector 11.

Although the embodiment shown in figure 1 is arranged for use in a multiband radiotelephone that supports both GSM and DCS, a person skilled in the art would appreciate that a more general PLL structure can be used, where, for example, the VCO 14 could be configured to provide an output frequency at the desired frequency without the need for a divider.

The phase locked loop 10 operates in the following manner, a reference signal, for example a 26 MHz signal, is feed to the phase detector 11. The phase

detector 11 compares the phase difference between the reference signal and an output signal from the N divider 17 to generate output pulses proportional to the error between the two phases of the signals. The output pulses from the phase detector 11 are used to either charge or discharge the charge pump 12, where the charge pump 12 has a first current output path and a second current output path, as described below. The signals between the phase detector 11 and the charge pump 12 are voltage signals.

The charge pump 12 charges or discharges the loop filter 13.

The loop filter 13 receives the current output from the first path and the second path and converts the current outputs, which reflect the phase difference between the two frequencies, into a voltage level, as described below. The voltage generated by the loop filter 13 is used to drive the VCO 14, where the VCO 14 is used to reduce the phase difference between the reference frequency and the output frequency of the N divider 17. The purpose of the first x2 divider 15, the second x2 divider 16 and the N divider 17 is to allow the generation of frequencies other than the reference frequency. As would be appreciated by a person skilled in the art by changing the N value it is possible to generate different frequencies, i.e. to act as a synthesizer. For example, the VCO 14 can be arranged, when the PLL 10 has locked to the 26 MHz reference frequency, to generate a 3.6 GHz signal, where the first x2 divider 15 converts the 3.6 GHz signal to a 1.8 GHz signal, suitable for DCS application. Correspondingly, the second x2 divider 16 converts the 1.8 GHz signal to a 0.9 GHz signal, suitable for GSM applications. The N divider 17 is arranged to convert the 0.9 GHz into a 26 MHz signal to maintain phase lock with the 26 MHz reference signal.

Figure 2 illustrates the loop filter 13 coupled to the first charge pump path 21 and the second charge pump path 22. The first charge pump path 21 and the second charge pump path 22 can either be formed from a single charge pump or two separate charge pumps. The first charge pump path 21 is arranged to have a

gain that corresponds to a charge pump gain I_{cp} divided by a factor B. The second charge pump path 22 is arranged to generate a second current that corresponds to the charge pump current I_{cp} minus the charge pump current I_{cp} divided by the factor B (i.e. $I_{cp} - I_{cp}/B$). However, other current relationships can be used between the first current pump path 21 and the second current pump path 22, however, to ensure that the overall capacitance of the loop filter is kept low it is highly desirable that the current generated on the first current pump path 21 be less than that of the current generated on the second current pump path 22.

The loop filter 13 comprises a parallel resistor/capacitor circuit 23 having a first resistive element R1 (for example, a resistor or an element having the same functionality such as a switched capacitor circuit or a MOS transistor operating in its linear region) in parallel with a first capacitor C1. The parallel resistor/capacitor circuit 23 is coupled at one end to a reference voltage, for example ground or other stable voltage, and at the other end to the second charge pump path 22 and, in series, to a second capacitor C2. The other end of the second capacitor C2 is coupled to the first charge pump path 21, thereby both the first charge pump path 21 and the second charge pump path 22 of the charge pump 12 provide a current simultaneously to the loop filter 13 for both frequency acquisition and locked mode.

For the purposes of this embodiment the loop filter 13 includes an additional pole created by a second resistive element R2 (for example, a resistor or an element having the same functionality such as a switched capacitor circuit or a MOS transistor operating in its linear region) coupled in series between the first charge pump path 21 and the VCO 14 and a third capacitor C3 that is coupled, at one end, between the second resistive element R2 and the VCO 14 and at the other end to a reference voltage, for example ground or other stable voltage. The purpose of the additional pole, created by the second resistive element R2 and third capacitor C3, is to further suppress phase noise and, though not essential, is a desirable feature.

The voltage formed across the second capacitor C2 corresponds to the integrated input current and is governed by the equation in the s-domain, as shown in figure 3:

$$V_B = \frac{I_{cp}}{B}\frac{1}{sC_2}$$

The voltage formed across the parallel resistor/capacitor circuit 23 corresponds to a low pass transfer with a pole ω_p and is governed by the equation, as shown in figure 3:

$$V_A = I_{cp}\left(R_1 \| C_1\right)$$

Consequently, the equivalent impedance of the loop filter can be calculated by:

$$\boxed{Z_{eq}(s) = \frac{V_A + V_B}{I_{cp}} = \frac{1}{sBC_2} \cdot \frac{1 + sR_1(BC_2 + C_1)}{1 + sR_1C_1}}$$

As the first capacitor C1 and the second capacitor C2 are placed in series this results in the voltages V_A and V_B being added, thereby combining the integrated voltage and the low pass transfer voltage. The resulting loop filter impedance and loop filter gain is shown in figure 3.

As the second capacitor C2 is used to integrate the input voltage, and correspondingly is used to form the required zero for the loop filter 13, using a factor B to divide the charge pump current I_{cp} provides the advantage of allowing the zero to be placed low enough, as illustrated in the filter impedance and loop gain graphs in figure 3, without requiring large capacitance values.

The choice of the value of B depends of several factors. If the value of B increases the overall capacitance decreases, as such if capacitance is an issue you may want to put B as high as possible. However, there are several upper limits to the value of B. First, when B increases the in-band phase noise increases at the same rate. Second, it has been found that for a passive dual path filter with an additional pole (i.e. R1/C2 in series with C1, followed by a R3/C2 pole) no mathematical solution exists when B reaches a value between 35 and 40, slightly depending on the loop parameters. Third, is the minimum current source that is practically achievable; if B increases, the auxiliary charge-pump gain decreases at the rate of 1/B. This can give extremely small current sources (lower than 1uA) that are difficult to control.

The low frequency path of the loop filter 13 formed between the first charge pump path 21 and the VCO 14 will, as a result of the charge pump current being divided by the factor B, be noisier than the high frequency path formed between the second charge pump path 22 and the VCO 14. However, as the bandwidth of the low frequency path is smaller than the loop filter bandwidth, as determined by the high frequency path, the additional noise generated on the low frequency path will have no impact on the out-of-band phase noise. In fact, as shown in figure 4, the noise generated by the low frequency path will be less than that of the high frequency path at offset frequencies higher than the loop filter bandwidth.

By way of example, using the above described loop filter, values for the first capacitor C1, the second capacitor C2, the third capacitor C3, the first resistive element R1 and the second resistive element R2 will know be calculated based on the following loop filter parameters:

Bandwidth 100kHz

KVCO = 400 MHz/V

Ref frequency 26 MHz

Dual Path ratio factor B = 30

Given the values of Icp, KVCO, ref. frequency, bandwidth and by solving the loop filter impedance equation $Z_{eq}(s)$ it is possible to obtain the appropriate values for the required capacitors and resistors. Consequently, utilizing the loop filter impedance equation for $Z_{eq}(s)$, as given above, with a first current pump path current of 20uA (i.e. 600uA /30) and a second current pump path current of 580 uA (i.e. 600uA – 20uA) the following components values can be calculated:

C2 = 90 pF

R1 = 1480 ohms

C1 = 225 pF

R2 = 4700 ohms

C3 = 300 pF

Therefore, the total loop filter capacitance for a loop filter based upon the loop filter described above is 615 pF.

This compares with a standard loop filter coupled to a single path charge pump where the corresponding component values would be:

C2 = 10 nF

R1 = 410 ohms

C1 = 880 pF

R2 = 1110 ohms

C3 = 300 pF

Therefore, the total loop filter capacitance for a single path loop filter is of the order of 11nF.

CLAIMS

1. A phase locked loop system comprising a charge pump (12) arranged to output a first current over a first charge pump path while a second current is output over a second charge pump path; and a phase locked loop filter (13) having a first capacitor (C2) electrically coupled to the first charge pump path; and a parallel resistor/capacitor circuit (23) electrically coupled to the second charge pump path with the resistor/capacitor circuit (23) having a second capacitor (C1); wherein the first capacitor (C2) and second capacitor (C1) are connected in series to allow a voltage associated with the first capacitor (C2) and a voltage associated with the parallel resistor/capacitor circuit (23) to be added together.

2. A phase locked loop system according to claim 1, wherein the current flow in the second path is greater than the current flow in the first path to allow a decrease in the capacitance of the phase locked loop filter (13).

3. A phase locked loop system according to claim 1 or 2, further comprising a third capacitor (C3) and a resistor (R2) to allow the generation of a pole.

4. A phase locked loop system according to any preceding claim, wherein the added voltage is arranged to control a voltage controlled oscillator (13).

5. An electronic device incorporating a phase locked loop system according to any preceding claim.

6. A radiotelephone incorporating a phase locked loop system according to any preceding claim.

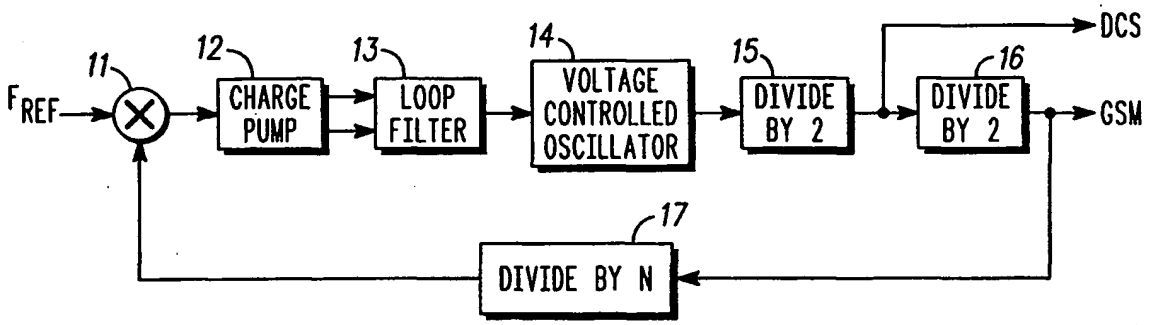

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FIG. 1

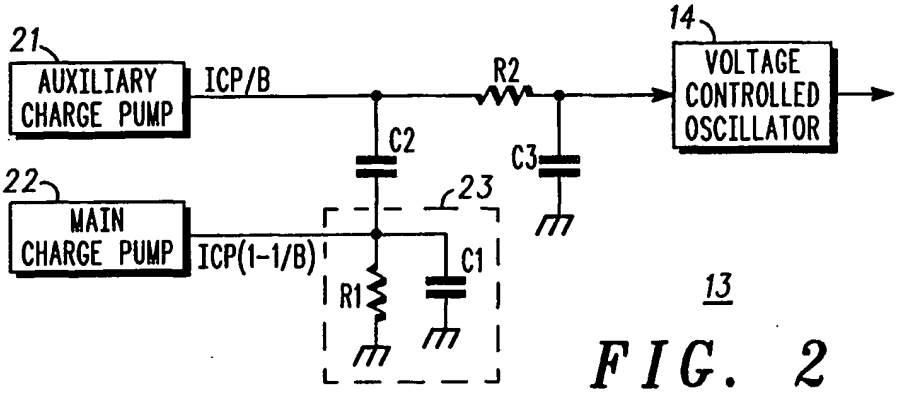

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FIG. 2

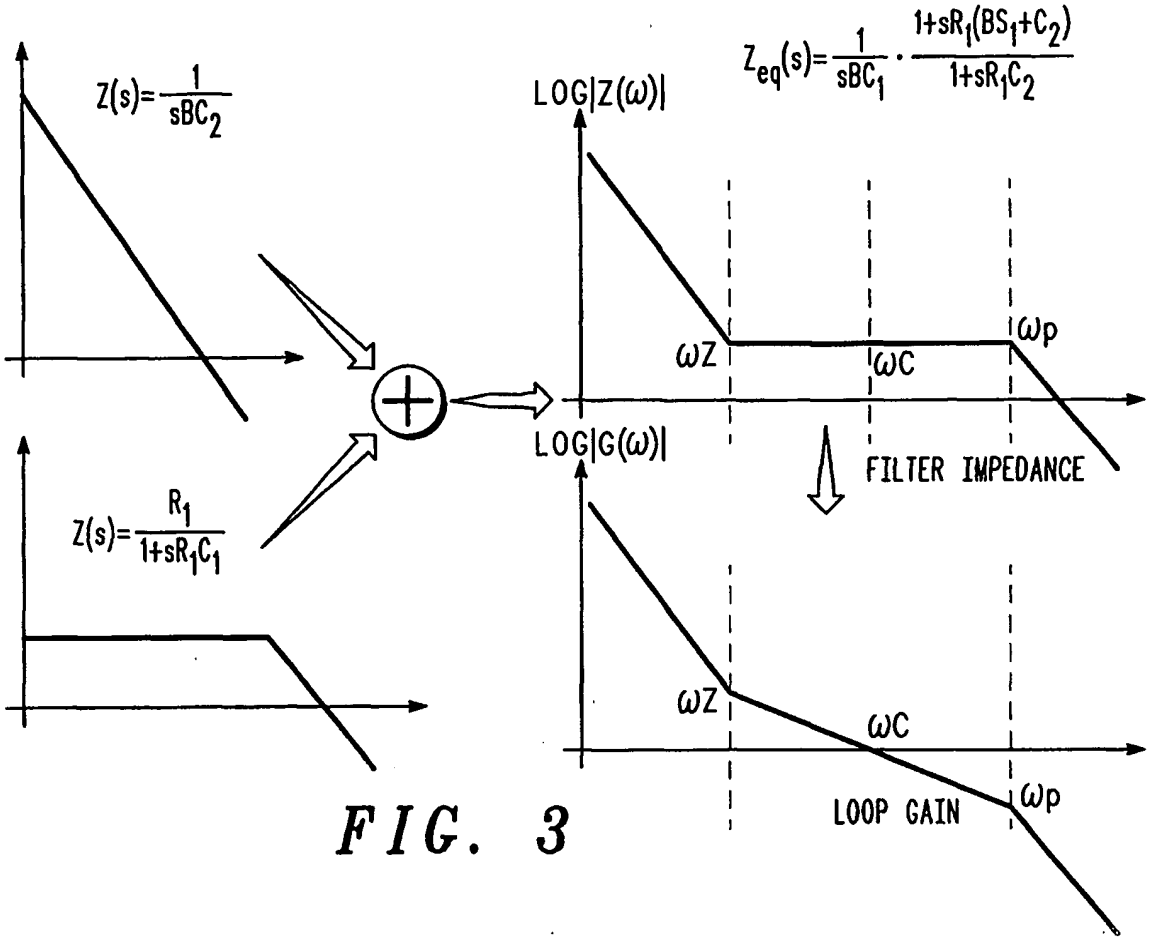
$Z(s)=\frac{1}{sBC_2}$
$Z(s)=\frac{R_1}{1+sR_1C_1}$
$Z_{eq}(s)=\frac{1}{sBC_1}\cdot\frac{1+sR_1(BS_1+C_2)}{1+sR_1C_2}$
LOG|Z(ω)|
LOG|G(ω)|
ωZ
ωC
ωp
FILTER IMPEDANCE
LOOP GAIN

FIG. 3

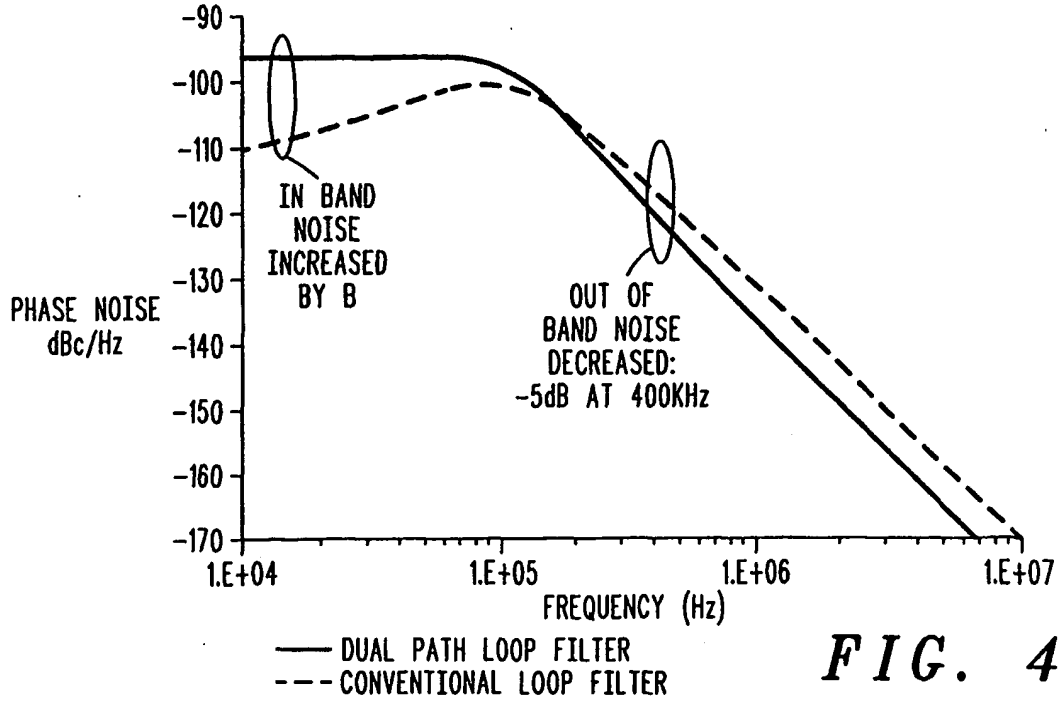
-90
-100
-110
-120
-130
-140
-150
-160
-170
PHASE NOISE dBc/Hz
IN BAND NOISE INCREASED BY B
OUT OF BAND NOISE DECREASED: -5dB AT 400KHz
1.E+04
1.E+05
1.E+06
1.E+07
FREQUENCY (Hz)
DUAL PATH LOOP FILTER
CONVENTIONAL LOOP FILTER

FIG. 4

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP2004/006481

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03L7/093 H03H7/01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 774 023 A (IRWIN JAMES STUART) 30 June 1998 (1998-06-30) cited in the application column 3, line 48 - column 4, line 26; figure 4	1-6
X	US 5 424 689 A (GILLIG STEVEN F ET AL) 13 June 1995 (1995-06-13)	1,2,4-6
A	column 3, line 31 - column 4, line 28 column 5, lines 5-67; claim 9; figures 4,8	3

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 October 2004	20/10/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Waters, D

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CRANINCKX J ET AL: "FULLY INTEGRATED CMOS DCS-1800 FREQUENCY SYNTHESIZER" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 33, no. 12, December 1998 (1998-12), pages 2054-2065, XP000880509 ISSN: 0018-9200 cited in the application page 2057, right-hand column, line 3 - page 2059, left-hand column, line 6; figures 9,10	1-6
X,P	US 2004/101081 A1 (HSU TSE-HSIANG) 27 May 2004 (2004-05-27)	1,2,4-6
A,P	abstract; figure 5	3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/EP2004/006481

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		GB 2285189 A ,B	28-06-1995
		IT RM940818 A1	22-06-1995
US 2004101081 A1	27-05-2004	TW 576023 B	11-02-2004